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Novel Technique on Channel Security using UART

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Abstract: This paper proposes a technique for implementing a UART (Universal Asynchronous receiver transmitter) with a new architecture such that the whole core can be modified for our desired specifications and can be integrated in a bigger design, wherever UART is necessary. This paper is implementing the design through Verilog HDL using Xilinx 14.2 design suite and it is tested on Spartan-6 FPGA after interfacing the circuit under test using PC with the help of RS-232 cable. The simulation results and the test results are supporting our proposal.

Keywords: UART, Verilog, FPGA, VLSI.

I. INTRODUCTION

It is always proved that the serial communication is superior to parallel communication in many aspects. One of the best ways to implement serial communication protocol is the Universal Asynchronous Receiver Transmitter. UART has been used in the on-board and on-chip networking, data exchange between computer and peripherals. As we all know that the exponential increase in the size of the systems being designed, has made an urge to come up with modular approaches. The ever increasing demand of the high speed data exchanges are being hindered by the increasing dynamic power consumption. So, this shows that one of the possible solutions to come up with, is the usage of asynchronous mode.

For these purposes, we designed an architecture, which allows us to modify and customize the specifications [1] and directly use it to fit the whole core into a bigger design.

The modifiable parameters include

1. System clock frequency (default-50MHz)
2. Baud rate
3. Number of parity bits (default 1)
4. Number of stop bits (1/1.5/2)
5. Oversampling factor (8/16)
6. The FIFO buffer parameters

II.EXISTING WORK

There are already few papers published on UART. The architecture required to build the complete core of the UART is adapted from [2]. The existing work dealt with the security providing purposes for serial communication through UART. The existing work which involves modifiable UART is not specific and rather generic, in the implementation manner. But here, in this paper, a novel approach for the implementation of architecture is proposed. This paper provides the comfort of adjusting all the above said parameters in a separate module, which is baud-rate generator module, without changing the top module.

III. ARCHITECTURE

Block Diagram of proposed UART module

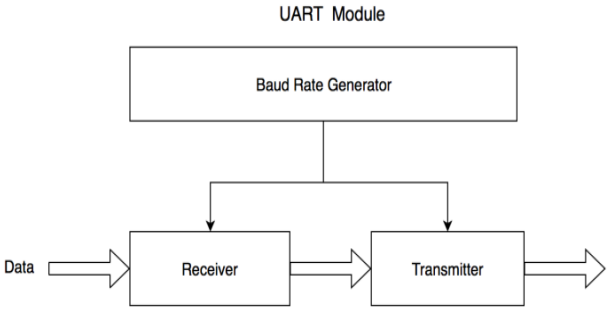

Fig. 1 Proposed UART Module.

The Fig. 1 has three modules. These three modules are Transmitter module, Receiver module and the baud rate generator module.

Paper Core Architecture

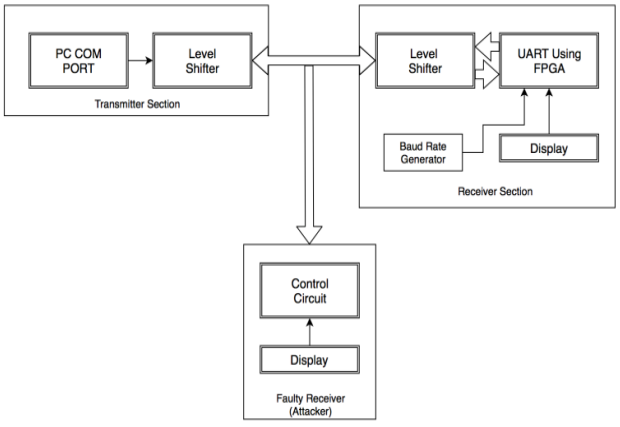

Fig.2 Core Architecture of UART.

The components from Fig. 2 are described as follows:

- Transmitter

The UART transmitter module is a simpler one to construct when compared to the UART receiver module.

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This is because there is no need of thinking about the synchronization at the transmitter. The over-sampling procedure is involved in the receiver, so the frequency if the ticks in transmitter are slower by the sampling factor than the receiver ticks. The byte transmitted by the transmitter contains the data bit, parity bit, stop bits.There are various application for serial transmission unit.

- Receiver

This is the hard part of implementation, as the serial data and the system clock are asynchronous; it is difficult to synchronize both. For this, it is important to detect the start bit of the frame received. Whenever an active low signal on the line is detected, then it is the start of the frame. For this, the over sampling procedure is used. For suppose, the sampling factor is 16, then the active low signal on line should at least last 8 ticks. So we count from 0 to 7, to make sure the start of frame is detected.

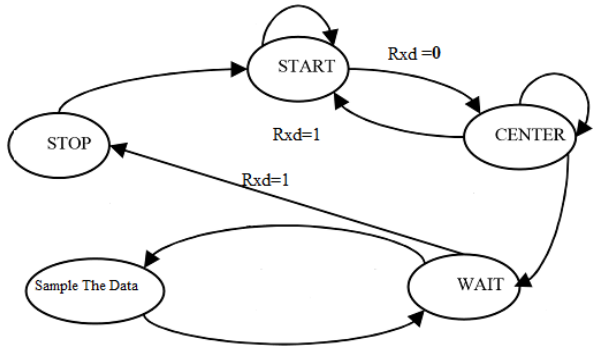

Fig.3 FSM State diagram for receiver.

By the time we reach the 8th tick, we would be in the middle of the received bit. So, after making sure that the frame has started, we again now reset the counter and start counting from 0 to 15, when we are at the 15th tick that means we are in the middle of the first data bit and it will be retrieved. Fig. 3 explains all these functions. The same procedure is followed until the whole frame is retrieved and stored in the FIFO buffer.

- Baud-rate generator

With the oscillator clock frequency and baud rate it is possible to calculate baud rate frequency which can be operated as divider factor. In this, obtained frequency clock is 16 times baud rate clock instead of equal clock frequency. So that it is possible to sample precisely asynchronous serial data at receiver. Expression for baud rate is given by, where M is frequency coefficient

Frequency Coefficient = Clock Frequency ÷
[(Sampling Rate) × (Baud rate)] (1)

M = (32MHz)÷ (16×9600Hz)
=208.

IV. COMPLETE UART CORE

The block diagram with complete UART core containing the baud rate generator, transmitter module, the receiver module and the FIFO buffers [3] is shown in the fig. 4.

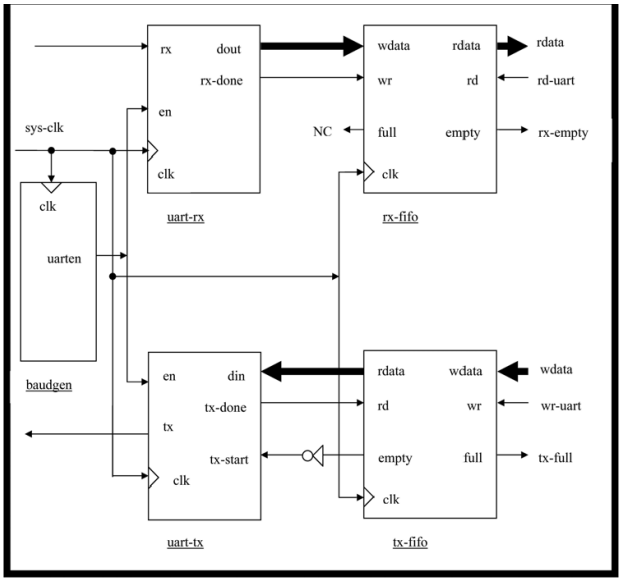

Fig. 4 Complete UART structure with various modules

V. RESULTS

The testing and simulation is done by the Xilinx Isim tool in the Xilinx ISE design suite. The simulation results for the designed block is presented in this section.

As it can be seen from the above figure, the data that is transmitted from the transmitter of the UART is being reflected in the received data.

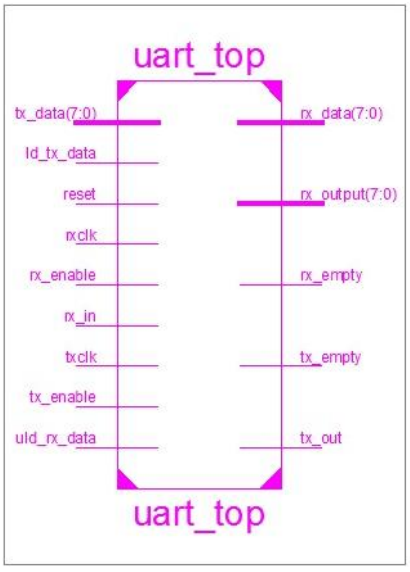

Fig.5 RTL Schematic of core module

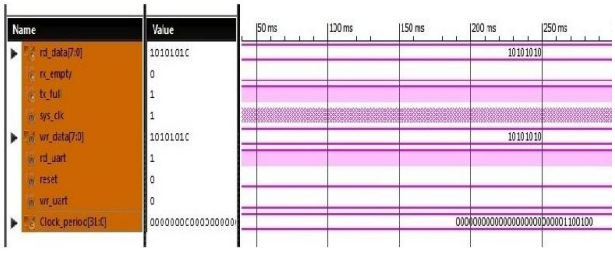

Fig.6 Simulation results of top core

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A. Testing

As per this paper approach, soon after logic check, designed module is tested practically by dumping logic HDL into FPGA kit of Spartan-3e family through RS232 cable. Then it is observed that designed model stores parallel data at receiver FIFO when it is received by UART model and again parallel data transmits to transmitter FIFO.

B. Area and Power

The utilities used are duly categorized and presented in the below table with all the percentages of their utilization. They have been calculated from the Xilinx XST Synthesizer which are not so significant and are as follows

Table.1 Device Utilization Summary.

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip Flops	42	1,536	2%
Number of 4 input LUTs	65	1,536	4%
Number of occupied Slices	50	768	6%
Number of Slices containing only related logic	50	50	100%
Number of Slices containing unrelated logic	0	50	0%
Total Number of 4 input LUTs	65	1,536	4%
Number of bonded IOBs	35	124	28%
Number of BUFGMUXs	2	8	25%
Average Fanout of Non-Clock Nets	3.32		

VI. APPLICATIONS

The UART has many applications in various fields of communication. The proposed architecture for modifiable UART sees its applications in any huge system where an UART is used and has desired specifications. In that case, the core can be modified with the desired specifications and can be integrated in the system. Some of the applications include

- Telecommunication synchronise routers
- Wide area mobile computing network.
- Router control.
- Cellular data transmission and reception.

VII. CONCLUSION

From various analyses, designed UART module operates fine with zero run error. And also possible to free from over run error by customizing under designed capability.The parameters were hanged and introspected for many cases and assured with desired results. The power parameters are calculated using XPowerAnalyzer [4]

Table.2 Power Analysis.

Name	Power (W)	Used	Total Available	Utilization (%)
Clocks	0.002	1	---	---
Logic	0.001	507	11776	4.3
Signals	0.003	665	---	---
IOs	0.008	7	372	1.9
Total Quiescent Power	**0.078**			
Total Dynamic Power	**0.014**			
Total Power	**0.092**			

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